WHAT IS CLAIMED IS:

1. A fraction frequency divider which divides an input signal by a frequency dividing number N/M of a ratio N/M of an integer M to N involving a decimal to output a frequency-divided signal, the divider comprising:

an integer setting section which sets an integer portion n of the frequency dividing number;

a decimal setting section which sets a decimal portion f of the frequency dividing number;

an accumulation/addition section including a decimal section which accumulates/adds a value of the decimal portion f in response to the outputted frequency-divided signal to provide a decimal value of an accumulation/addition result and an integer section to provide a carry signal;

an adder which adds the value of the integer portion n of the integer setting section and the value of the integer portion of the accumulation/addition result;

a dividing section which switches the frequency dividing number to a result obtained by the adder to divide the input signal and which outputs the frequency-divided signal;

a dividing number setting section which sets a number Mn of n-dividing operations to be performed, and a number Mn+1 of n+1-dividing operations to be

performed, these numbers being obtained from a relation of the integers M, N, and n;

a counter section including a first counter which counts the number of performed n-dividing operations in response to the frequency-divided signal and a second counter which counts the number of performed n+1-dividing operations in response to the frequency-divided signal based on the carry signal of the integer section of the accumulation/addition section; and

a calculation processing section which sets the integer portion of the accumulation/addition result to one of 0 and 1 in accordance with a content of one of the first and second counters and which resets the first and second counters and the accumulation/addition section in accordance with the content of the other of the first and second counters and which sets the contents of the counters and the accumulation/addition section to 0.

2. The fraction frequency divider according to claim 1, wherein the calculation processing section sets the integer portion of the accumulation/addition result to 1, when the content of the first counter is Mn, and resets the first and second counters and the accumulation/addition section and sets the contents of the counters and the accumulation/addition section to 0, when the second counter indicates Mn+1.

3. The fraction frequency divider according to

claim 1, wherein the dividing number setting section obtains the number Mn of n-dividing operations to be performed and the number Mn+1 of n+1-dividing operations to be performed by the following equations:

$N/M = n.f$;

$M = Mn + Mn+1$; and

$N = Mn \times n + Mn+1 \times (n+1)$, where n denotes an integer and f denotes a decimal numeric value.

4. The fraction frequency divider according to claim 2, wherein the dividing number setting section obtains the number Mn of n-dividing operations to be performed and the number Mn+1 of n+1-dividing operations to be performed by the following equations:

$N/M = n.f$;

$M = Mn + Mn+1$; and

$N = Mn \times n + Mn+1 \times (n+1)$, where n denotes an integer and f denotes a decimal numeric value.

5. A large scale integration circuit for a video signal, comprising: a phase lock loop circuit which uses a phase lock loop to produce an audio clock for digital/analog-converting audio data from a video clock separated from an inputted composite video signal,

wherein the phase lock loop circuit includes a frequency divider which divides an input clock signal, and

the frequency divider divides an input signal by a frequency dividing number N/M of a ratio N/M of

an integer M to N involving a decimal to output a frequency-divided signal, and comprises:

an integer setting section which sets an integer portion n of the frequency dividing number;

a decimal setting section which sets a decimal portion f of the frequency dividing number;

an accumulation/addition section including a decimal section which accumulates/adds a value of the decimal portion f in response to the outputted frequency-divided signal to provide a decimal value of an accumulation/addition result and an integer section to provide a carry signal;

an adder which adds the value of the integer portion n of the integer setting section and the value of the integer portion of the accumulation/addition result;

a dividing section which switches the frequency dividing number to a result obtained by the adder to divide the input signal and which outputs the frequency-divided signal;

a dividing number setting section which sets a number Mn of n-dividing operations to be performed, and a number Mn+1 of n+1-dividing operations to be performed, these numbers being obtained from a relation of the integers M, N, and n;

a counter section including a first counter which counts the number of performed n-dividing operations

in response to the frequency-divided signal and a second counter which counts the number of performed n+1-dividing operations in response to the frequency-divided signal based on the carry signal of the integer section of the accumulation/addition section; and

a calculation processing section which sets the integer portion of the accumulation/addition result to one of 0 and 1 in accordance with a content of one of the first and second counters and which resets the first and second counters and the accumulation/addition section in accordance with the content of the other of the first and second counters and which sets the contents of the counters and the accumulation/addition section to 0.

6. The large scale integration circuit for the video signal according to claim 5, wherein the calculation processing section sets the integer portion of the accumulation/addition result to 1, when the content of the first counter is Mn, and resets the first and second counters and the accumulation/addition section and sets the contents of the counters and the accumulation/addition section to 0, when the second counter indicates Mn+1.

7. A method of dividing an input signal by a frequency dividing number of a ratio N/M of an integer M to N involving a decimal to output a frequency-divided signal, the method comprising:

setting an integer portion n of the frequency dividing number;

setting a decimal portion f of the frequency dividing number;

accumulating/adding a value of the decimal portion f in response to the frequency-divided signal to provide a decimal value of an accumulation/addition result as a decimal portion and to provide a carry signal as an integer portion;

adding the value of the set integer portion n and the value of the integer portion of the accumulation/addition result to provide an added value of an integer;

using the added value of the integer as a frequency dividing number to divide the input signal;

setting a number Mn of n-dividing operations to be performed, and a number Mn+1 of n+1-dividing operations to be performed, obtained from a relation of the integers M, N, and n;

counting the number of performed n-dividing operations in response to the frequency-divided signal by a first counter, and counting the number of performed n+1-dividing operations in response to the frequency-divided signal by a second counter based on the value of the integer portion of the accumulation/addition result; and

fixing the integer portion of the

accumulation/addition result to 1, when the number of performed n-dividing operations is Mn, and resetting the first and second counters and the decimal portion and integer portion of the accumulation/addition result and setting the contents of the counters and the accumulation/addition section to 0, when the number of performed n+1-dividing operations is Mn+1.